Power integrity electromagnetic analysis for printed circuit boards (PCB) using the finite element method (FEM)

In the design of a PCB, one of the fundamental elements for the correct operation of the system is the Power Distribution Network (PDN) of the various integrated circuits assembled on the board, consisting mainly of power rails and ground rails. If the network is not designed correctly, malfunctions and/or electromagnetic compatibility issues may occur, such as radiated emissions or susceptibility to RF interference.

The circuit under analysis consists of the following key components:

- **Voltage Regulating Module (VRM).** The component that powers the system, which must be able to supply the current necessary for the board to function correctly at the various voltages required
- **Sinks.** The integrated circuits, such as CPUs and FPGAs, that demand a significant amount of current for the correct operation of the board
- **Power Rail.** The part of the power distribution network that carries the operating voltage from the regulating module to the sink
- **Ground rail.** The part of the circuit that closes the current loop from the sink to the regulating module

In this article we describe a series of analyses conducted on an embedded PCB in COM Express format, a widely popular, high-performance and compact industrial format, developed by the SECO Srl company based in Arezzo, Italy. The main component of the board is an AMD R-Series (Merlin Falcon) processor (3.2 GHz max.) working with a peak maximum supply current of around 51 A on the vcore in performance mode and therefore requires careful design of the power rail. The new Keysight Technologies PIPro simulator was used for the power integrity analysis. This simulator is based on electromagnetic analysis using the finite element method (FEM) and optimised to facilitate quick and accurate analysis of medium to large boards with a high number of layers. The figure below shows the routed board after it was imported into the Advanced Design System software of Keysight EEsof EDA.
Below is a detailed diagram of the main power rail for the CPU (1.2 V), excluding grounds, with the Z-axis scale increased for improved visibility of the circuit. Note the top left area in blue, where the CPU is connected, and the bottom right, where the voltage regulating module is connected.
We start with the simplest analysis (PI-DC), which involves calculating static DC voltage drops and associated power and current densities throughout the PDN. This analysis allows us to identify the main integrated circuits, connector pins and ground stitching vias which carry the highest amount of current.

If the voltage in the power distribution network drops below a set value, the integrated circuit will not reach the minimum voltage level required for its correct operation and the circuit will either shut down, reset itself, or the internal logic of the device will malfunction. Excessive current densities in the power distribution network can create high temperatures that can cause delamination of the printed circuit board and, in cases of extreme overheating, the board can even catch fire. Vertical Interconnect Accesses (vias) carrying excessive currents can melt and interrupt the circuit.

Static direct current simulation (PI-DC) generates various results, including those shown in the figure below. Here you can see that the minimum voltage in the area where the CPU is connected reaches a minimum value of around 1.1 V, including the maximum tolerance of ±120 mV, compared with a nominal operating voltage of 1.2 V for the CPU.

![Voltage Simulation Image]

A detailed report is also available, including quantitative voltage measurements both for the CPU (see figure below) and for the regulating module, as well as current and voltage measurements on the connection pads and in the vias, indicating where set maximum values are exceeded.
The purpose of the second type of analysis (PI-AC) is to ensure that the minimum operating voltage level is maintained in dynamic conditions, i.e. once the device is in operation and its power consumption varies over time according to the type and sequence of operations executed by the CPU. The frequency of the R-Series processor clock is 3.2 GHz, so the current signal on the supply rail has a high harmonic content. As a result, the electromagnetic simulation of the power circuit is configured to cover the entire spectrum from DC to 3 GHz. Equivalent models of the voltage regulator, sink and decoupling capacitors are then automatically added to the model obtained. The decoupling capacitors are connected between the power and ground rails and their positioning and capacity values constitute the main parameters available to the designer to optimize system operation. From an operating point of view, the principal findings of the complete simulation can be seen in the diagram shown below, in which the impedance value measured by the CPU (axis Y) is compared with the frequency (axis X), both on a logarithmic scale.
Two curves are marked on this diagram, one with the decoupling capacitors disconnected (red curve) and the other with the capacitors connected. The models used for the capacitors include the parasitic elements of inductance and resistance and can be defined through S-parameter models. Note how the general impedance value in the second case is lower and how the resonance peak is reduced in size (around 22 Ohm to around 5 Ohm) and shifted to an upper frequency (from around 230 MHz to more than 900 MHz).

In this case, there are no accurate details available on the maximum impedance level permitted relative to the frequency, and therefore a target impedance was calculated from the relationship between the maximum ripple voltage permitted and the maximum transient current set by the CPU manufacturer, which gave a value of around 150 mOhm. This value is maintained up to 100 MHz, after which frequency the design goal in this case is to move any resonance as high in frequency as possible.

The final power integrity analysis conducted involves mapping power plane resonances on the board (Power Plane Resonance analysis, PI-PPR), which facilitates the subsequent addition of any decoupling capacitors in optimal positions to suppress residual resonances.
In the figure above you can see the distribution of the electric field at the principal resonance frequency, where the coloured zones in red correspond to the location of resonances on one of the ground planes.

Conducting these analyses and making the necessary improvements rapidly brought the board back to within the impedance specifications established during the project. Use of the PIPro simulator, given its speed (the longest simulation lasted around 1 hr 15 min) and accuracy, saved time during the design process and enabled a quick transition to the board manufacturing phase.